

FIG. 1A

(PRIOR ART)

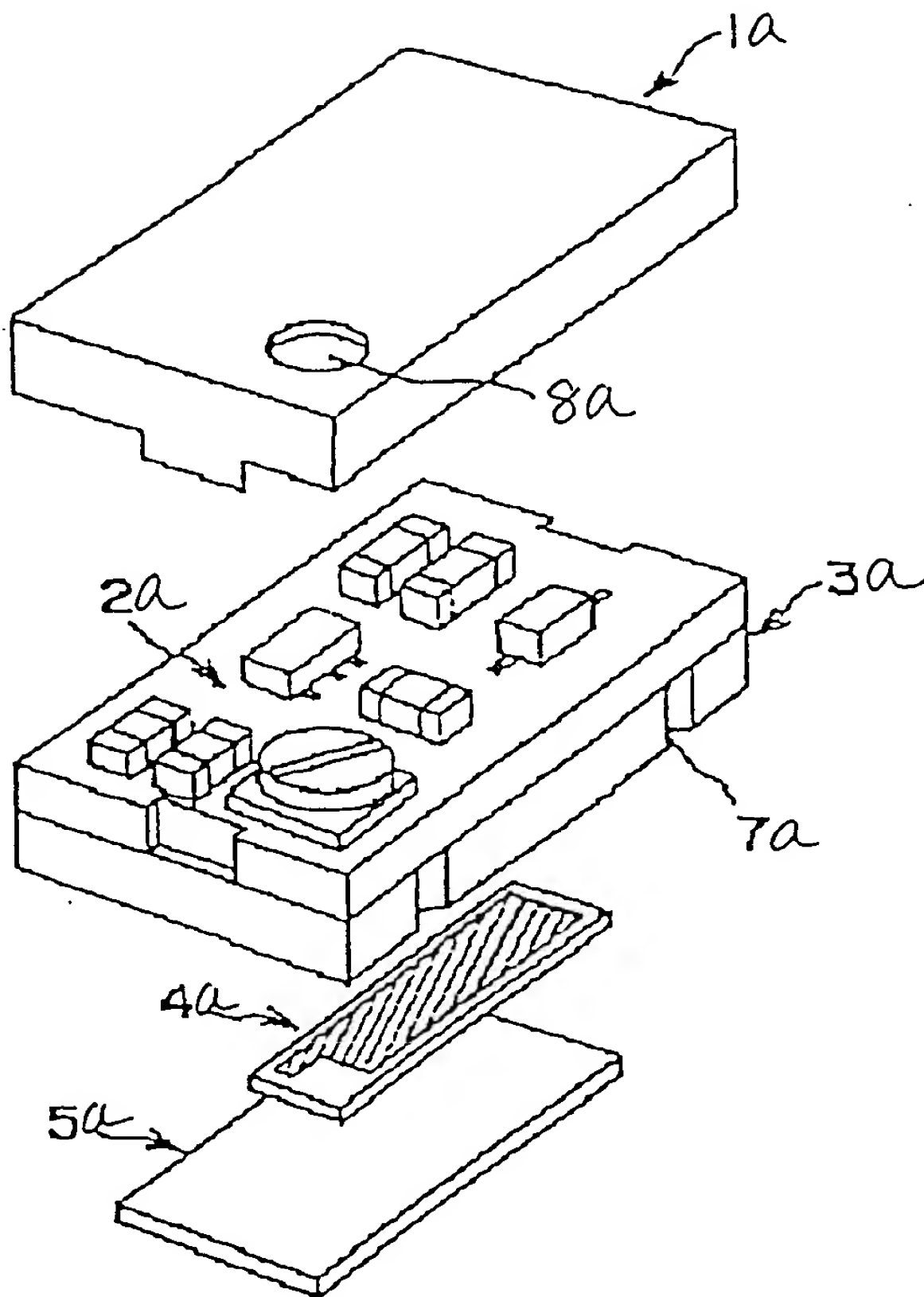


FIG. 1B

(PRIOR ART)

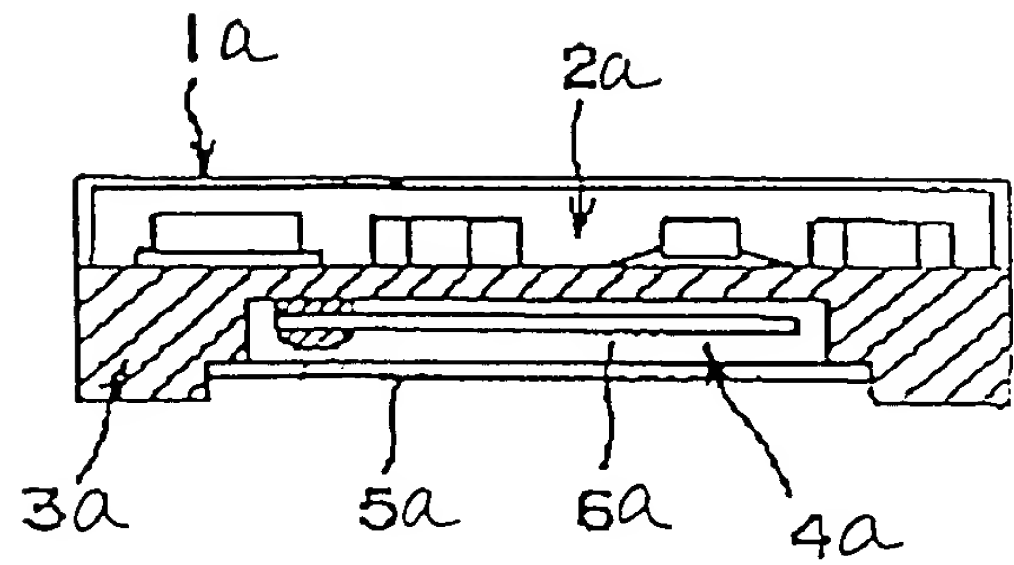


Diagram 1b is a cross-sectional view of a second embodiment of the semiconductor device. It shows a similar structure to the first embodiment, with a substrate 1b and a gate stack 2b. The gate stack 2b includes a gate insulating layer 4b, a gate electrode 5b, and a gate insulating layer 6b. A second conductive layer 7b is formed on the gate electrode 5b. A second semiconductor layer 8b is formed on the gate stack 2b. A second source/drain region 9b is formed in the second semiconductor layer 8b. A second contact layer 15b is formed on the second source/drain region 9b. The second conductive layer 7b is connected to the second source/drain region 9b through a second contact layer 15b.

FIG. 3

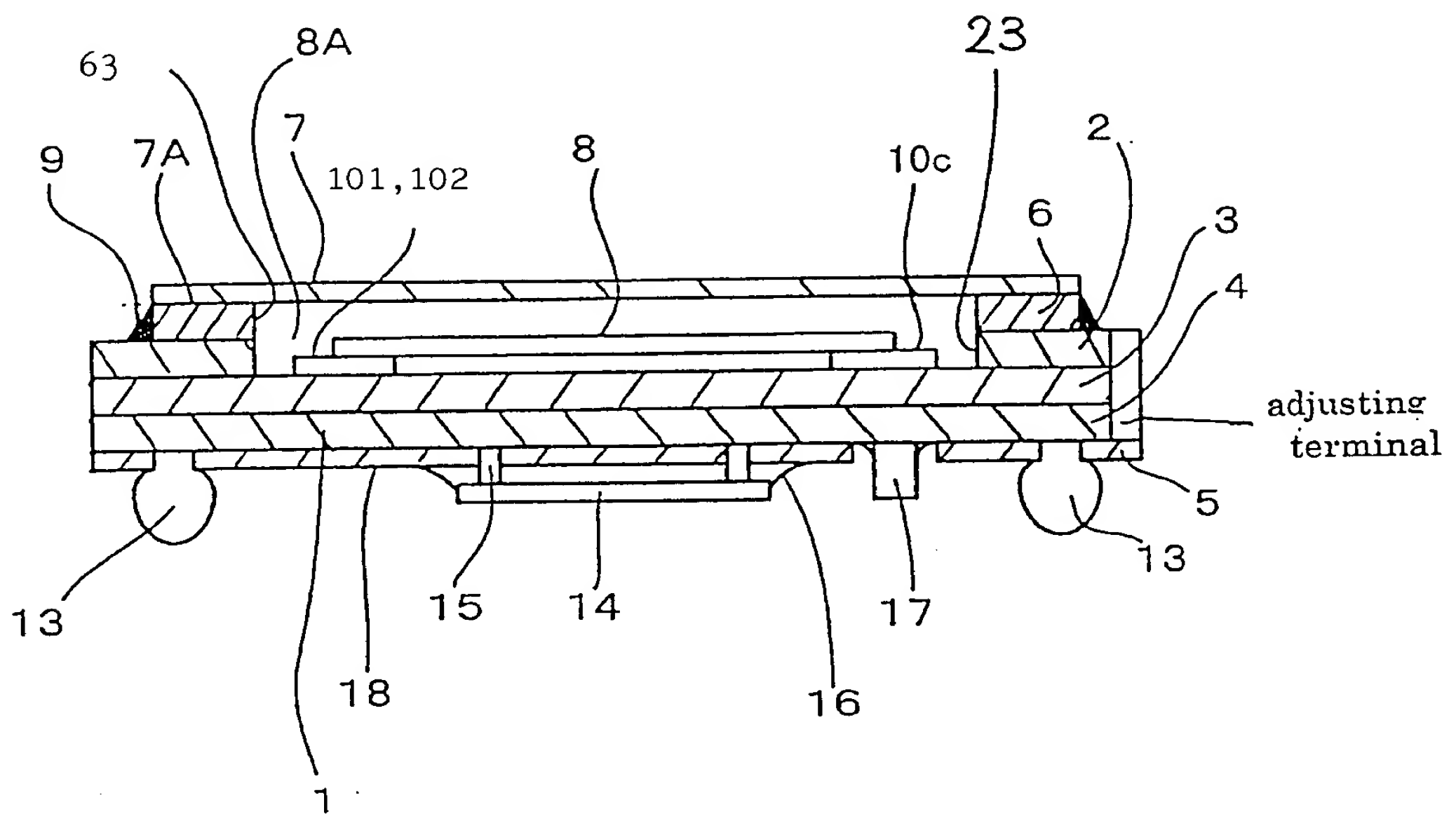


FIG. 4

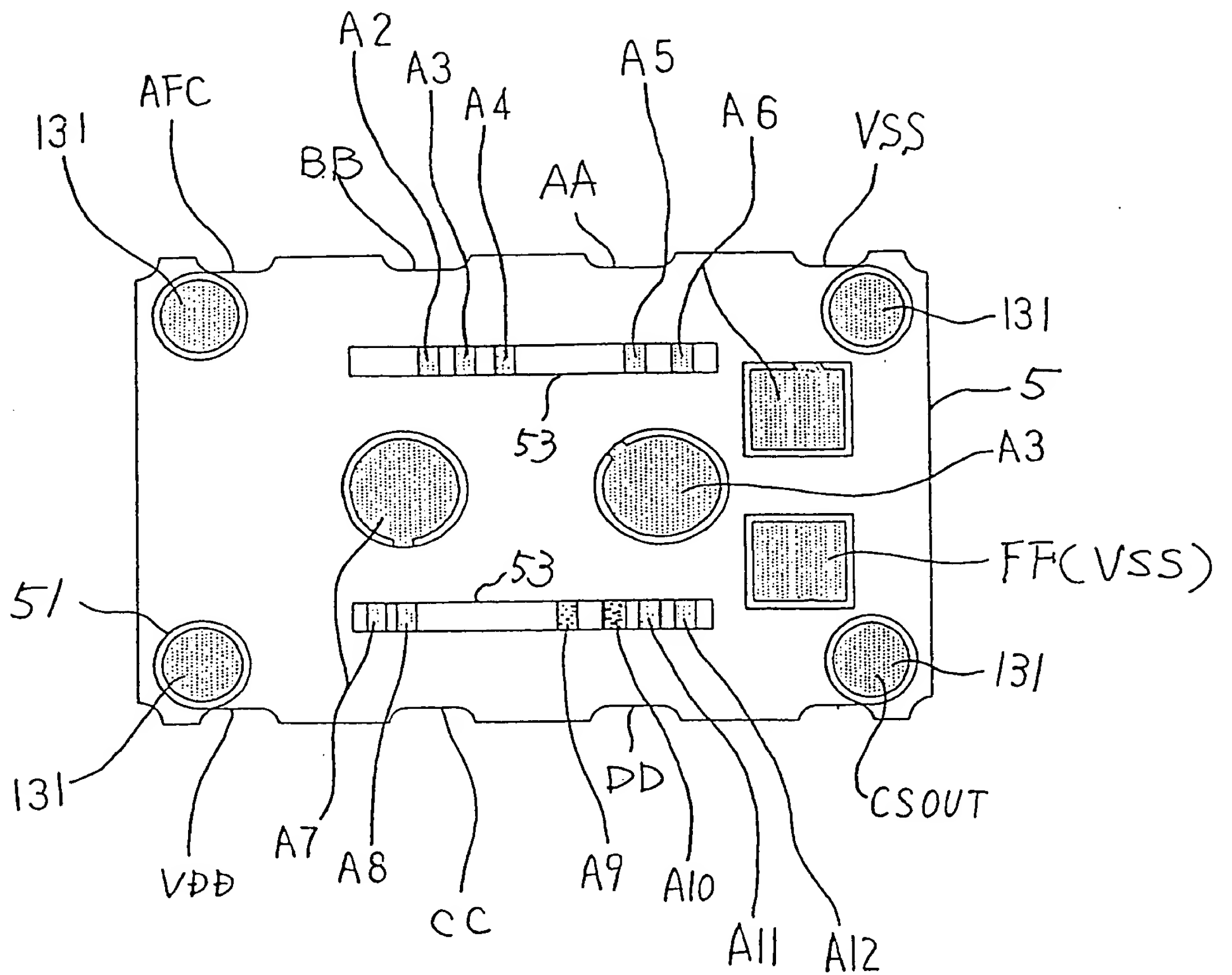


FIG. 5

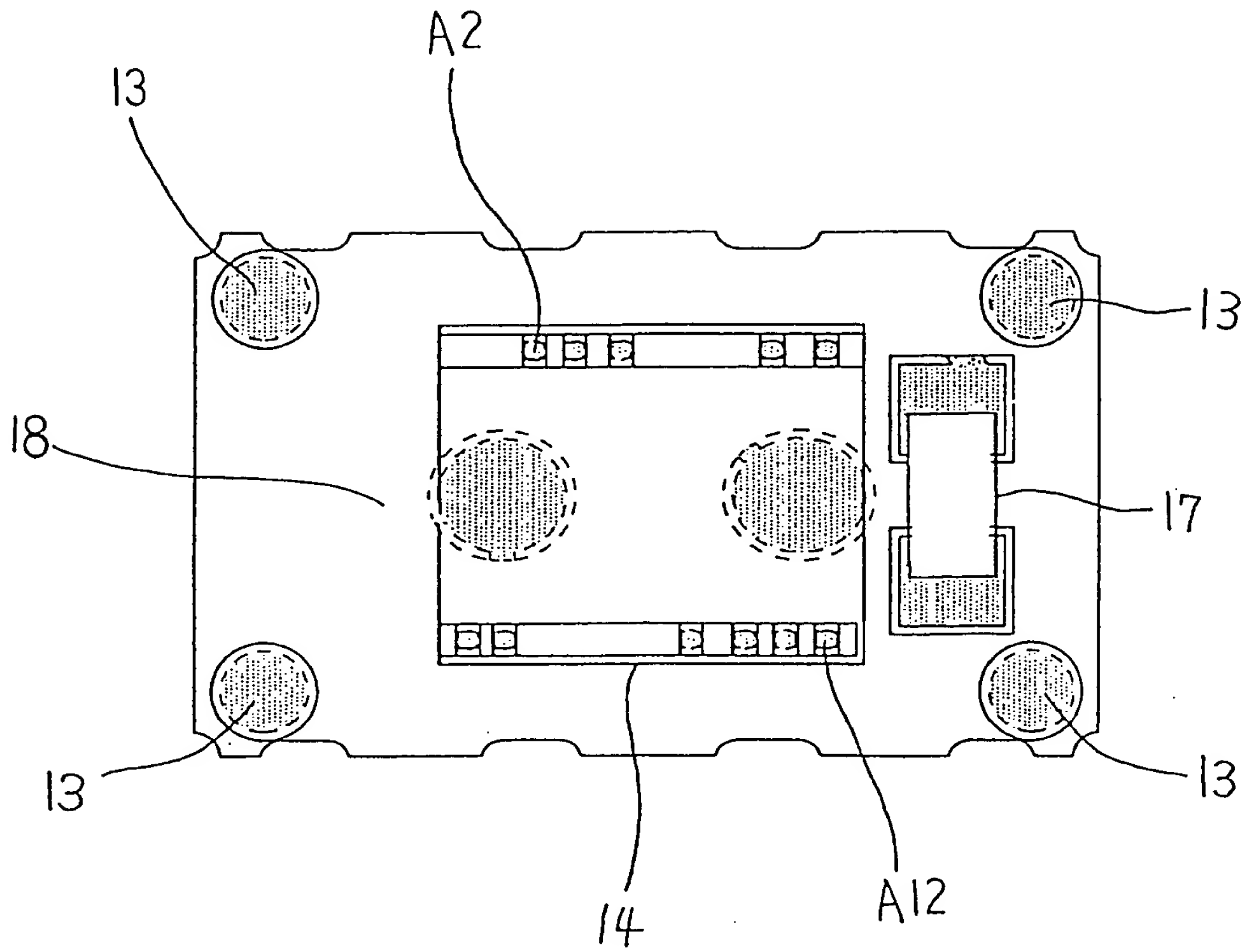


FIG. 6

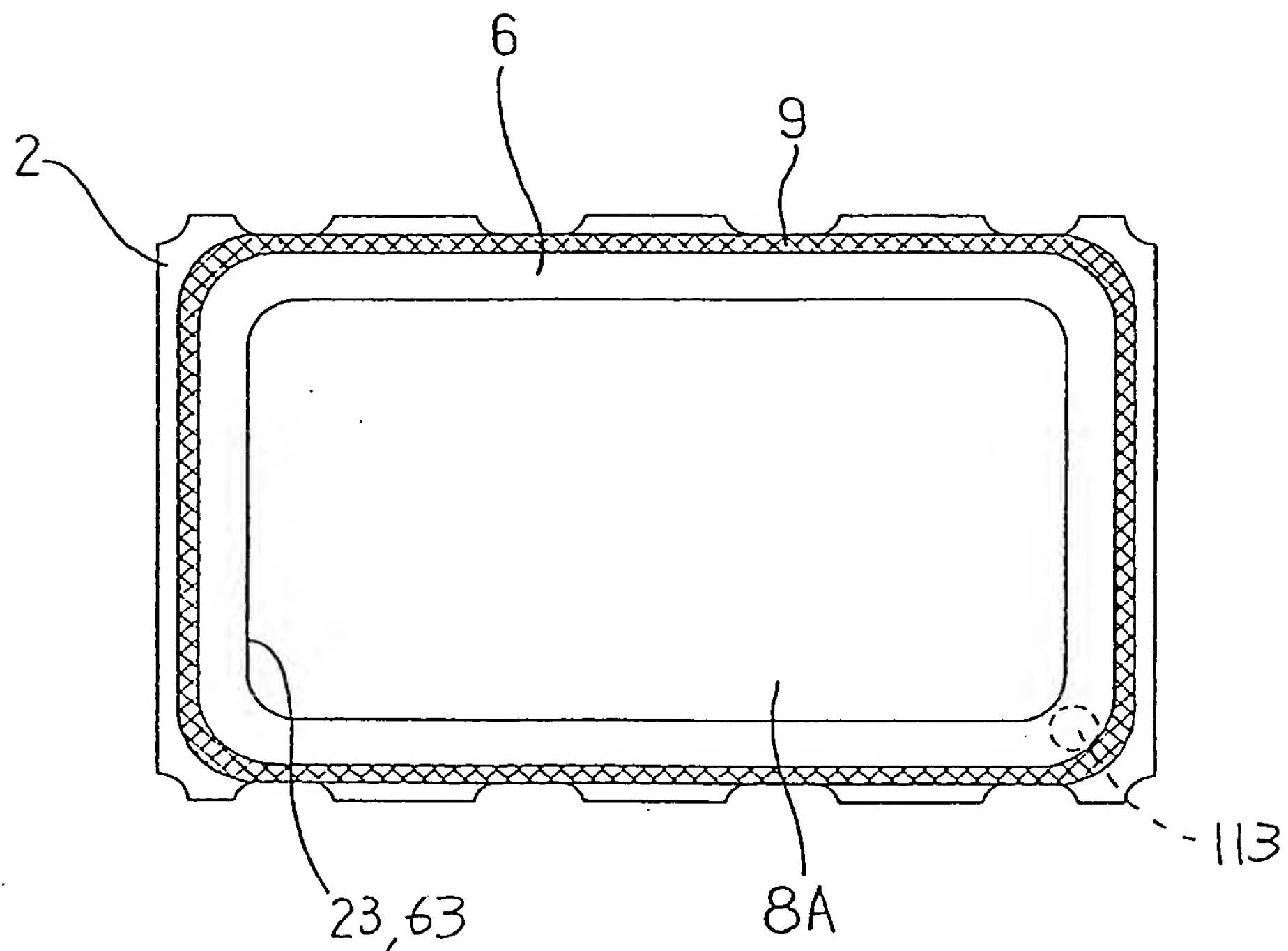


FIG. 7

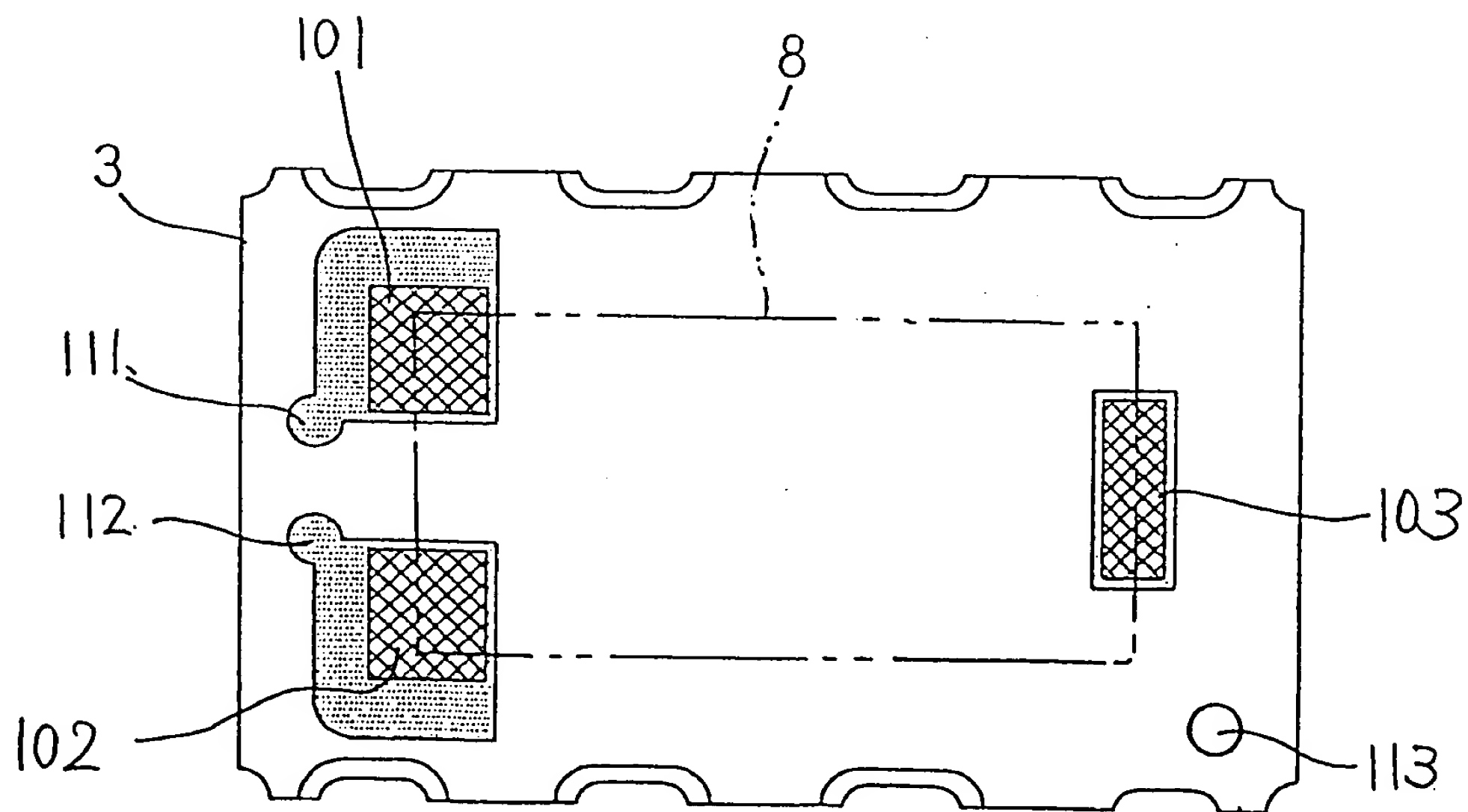


FIG. 8

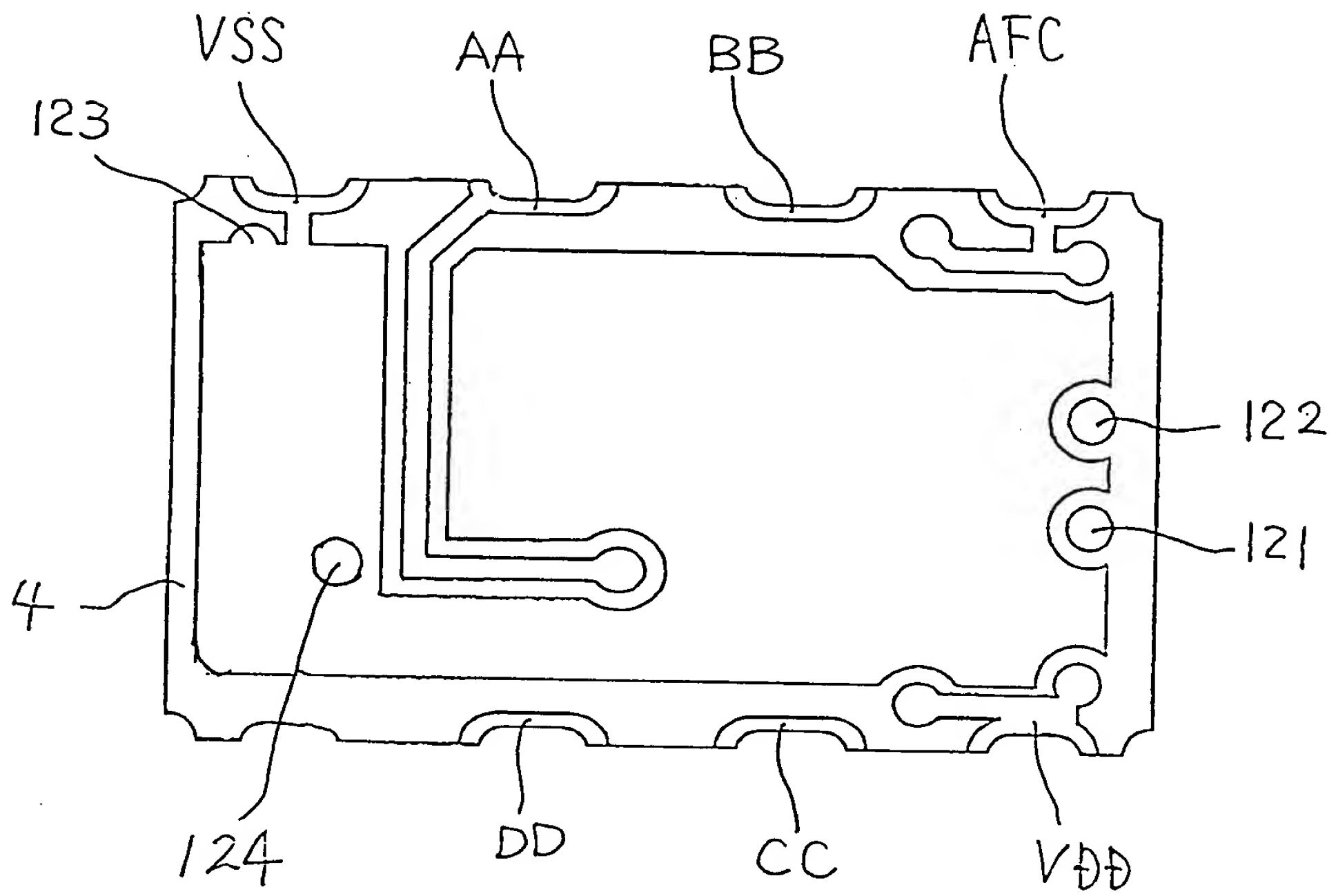


FIG. 8

FIG. 9

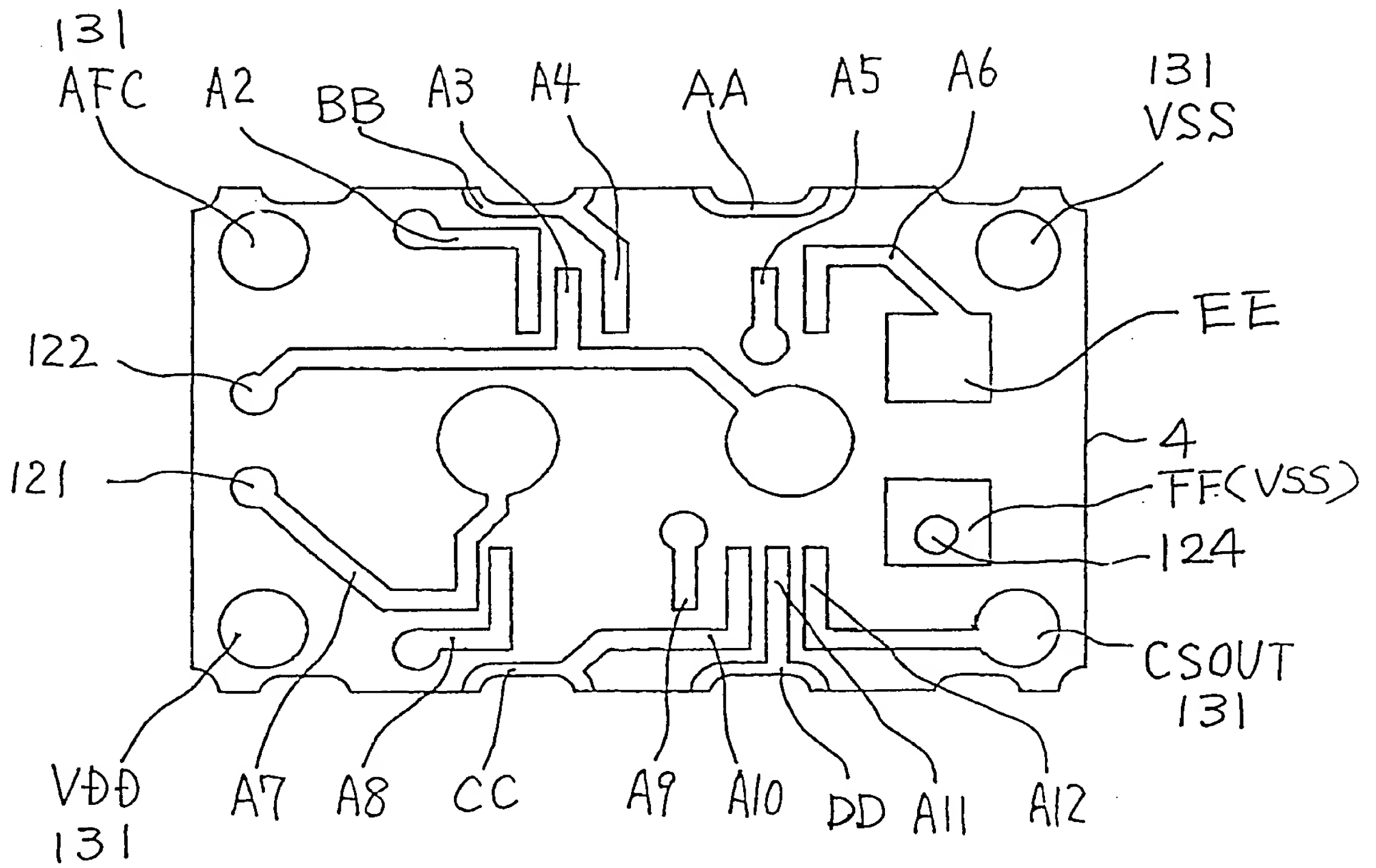


FIG. 10

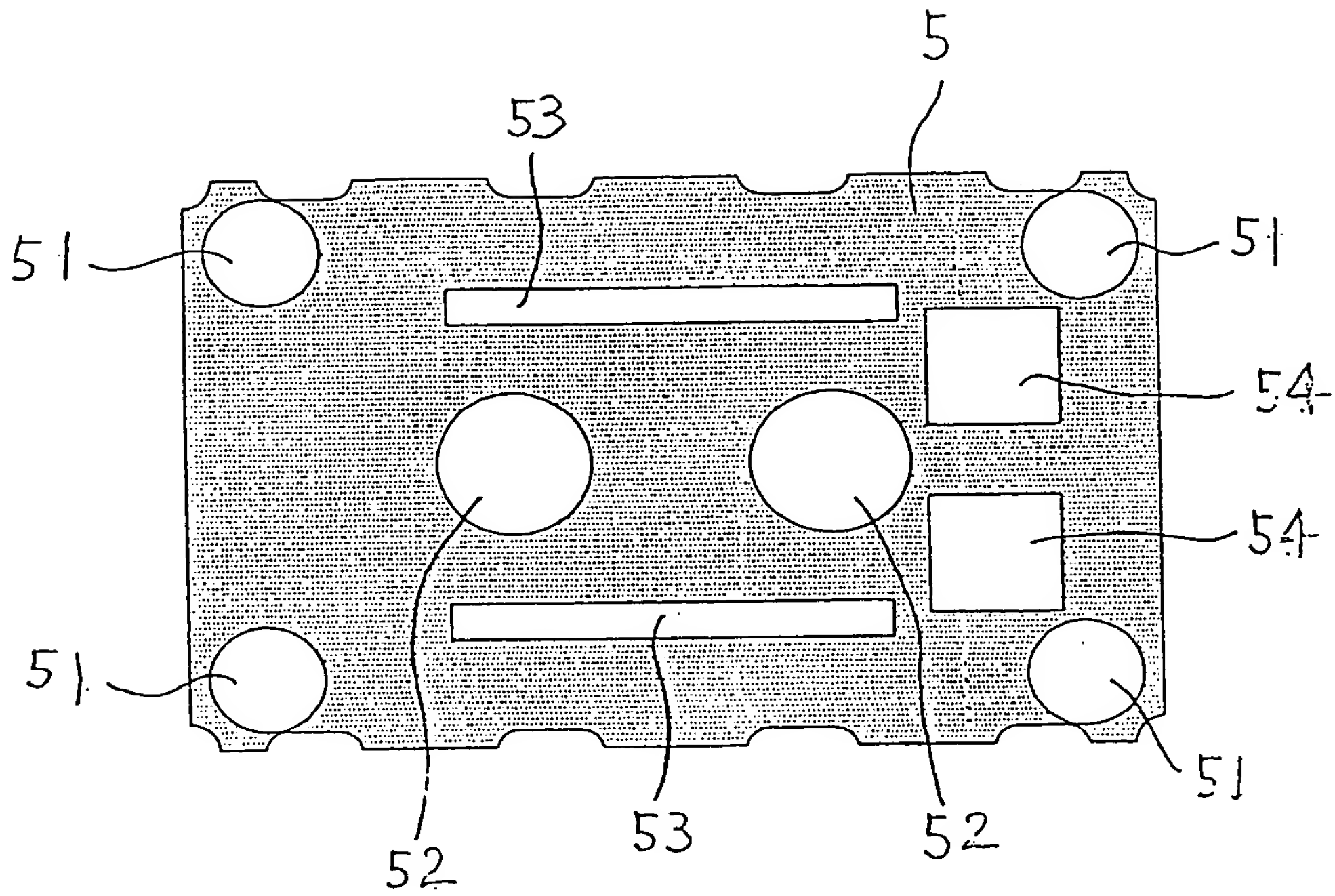


FIG. 11

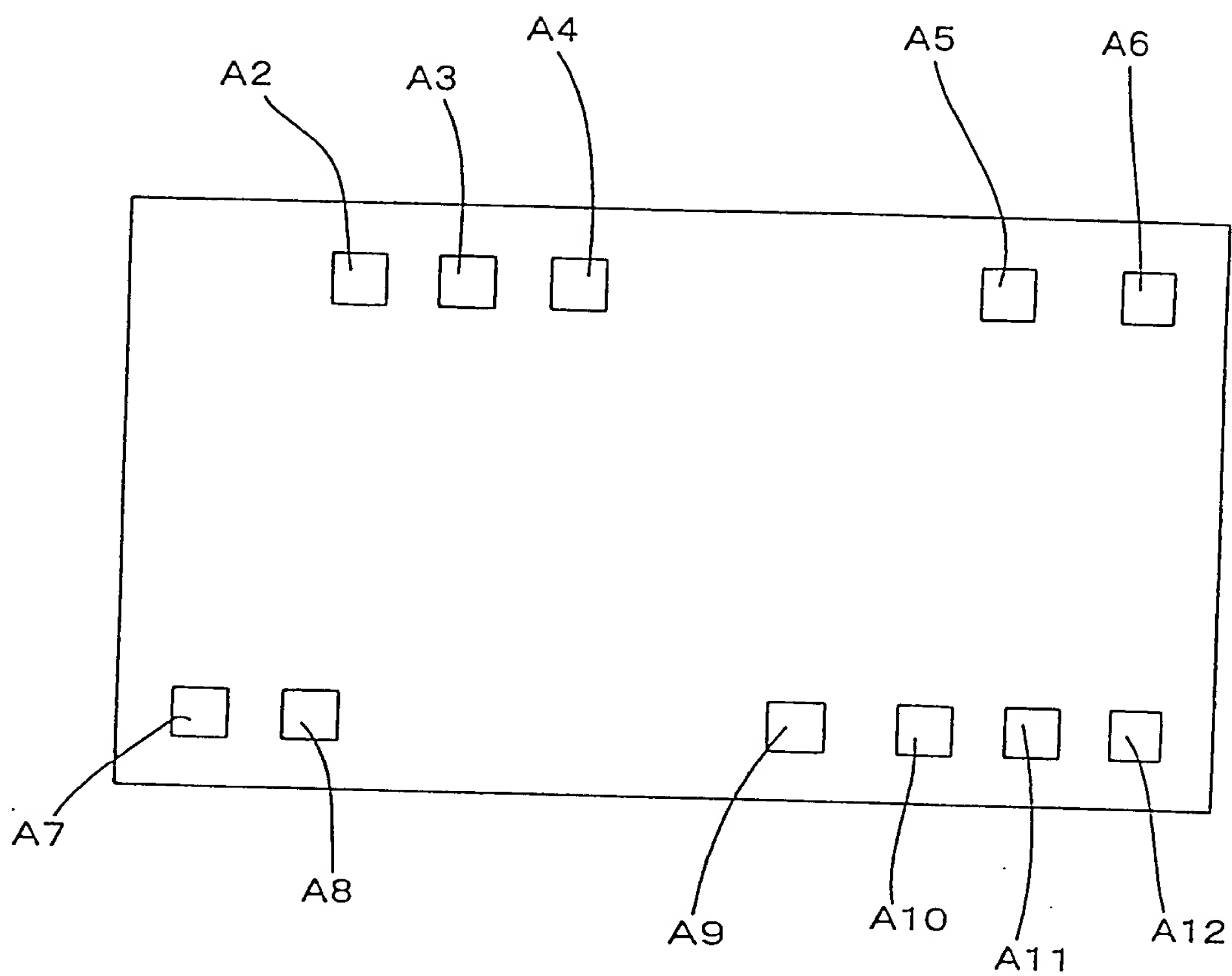


FIG. 12

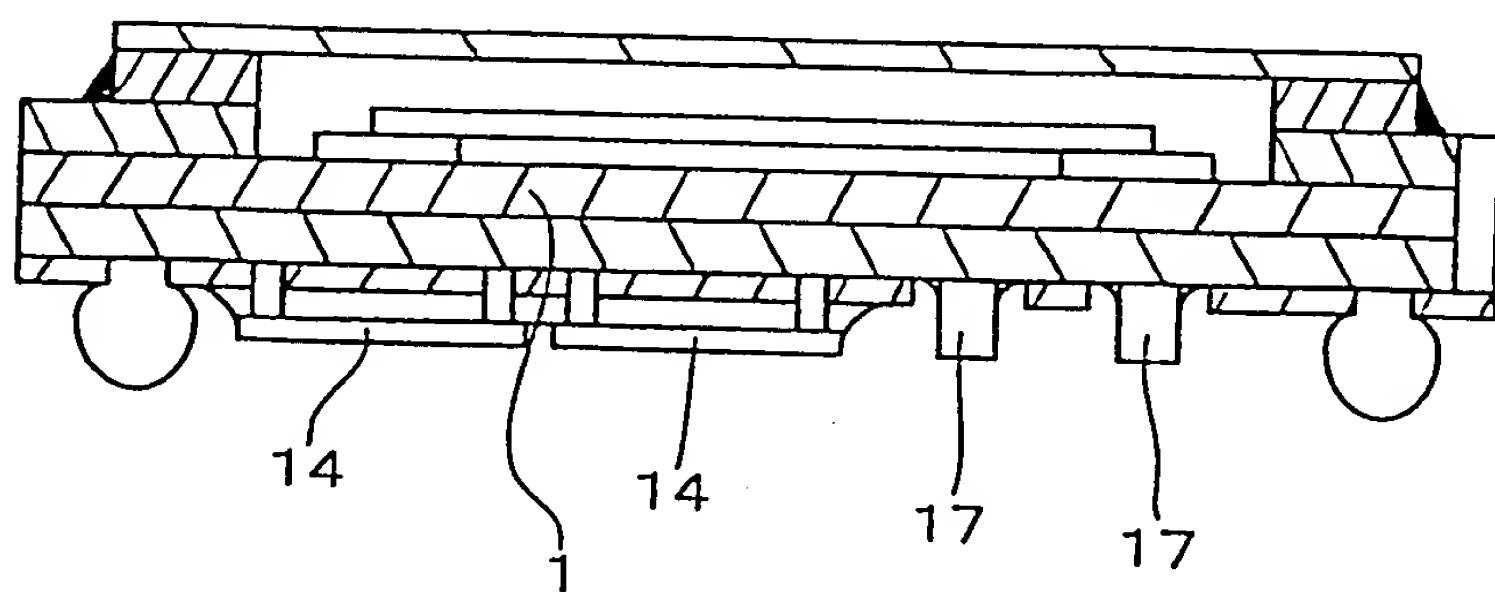


FIG. 13

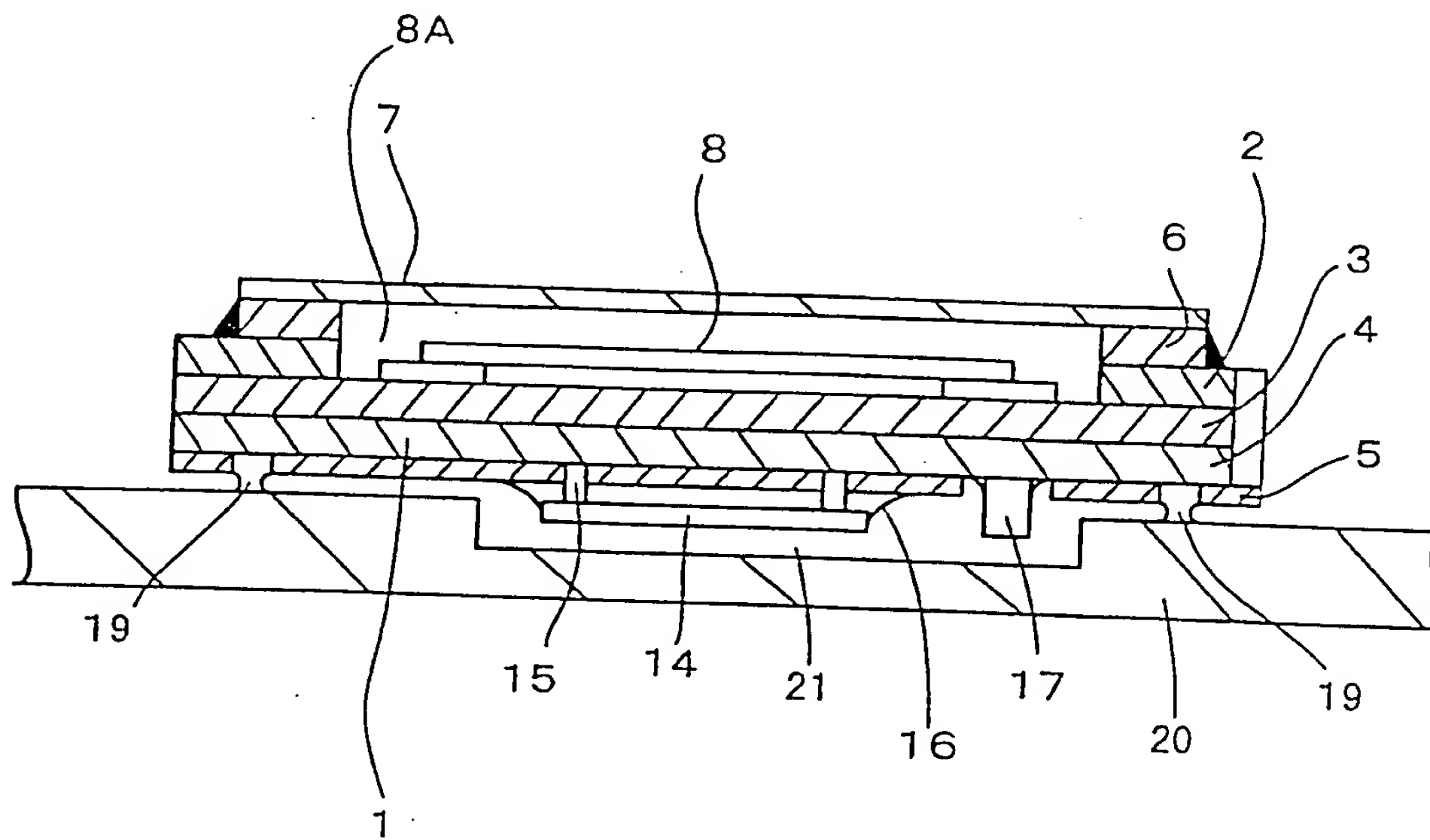


FIG. 14

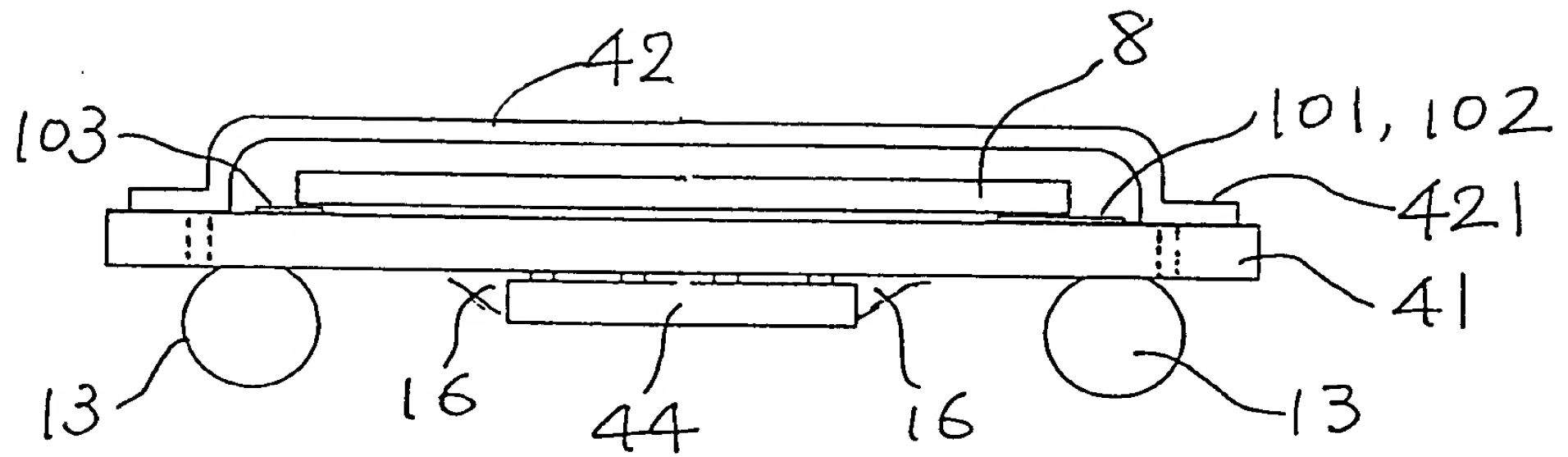


FIG. 15

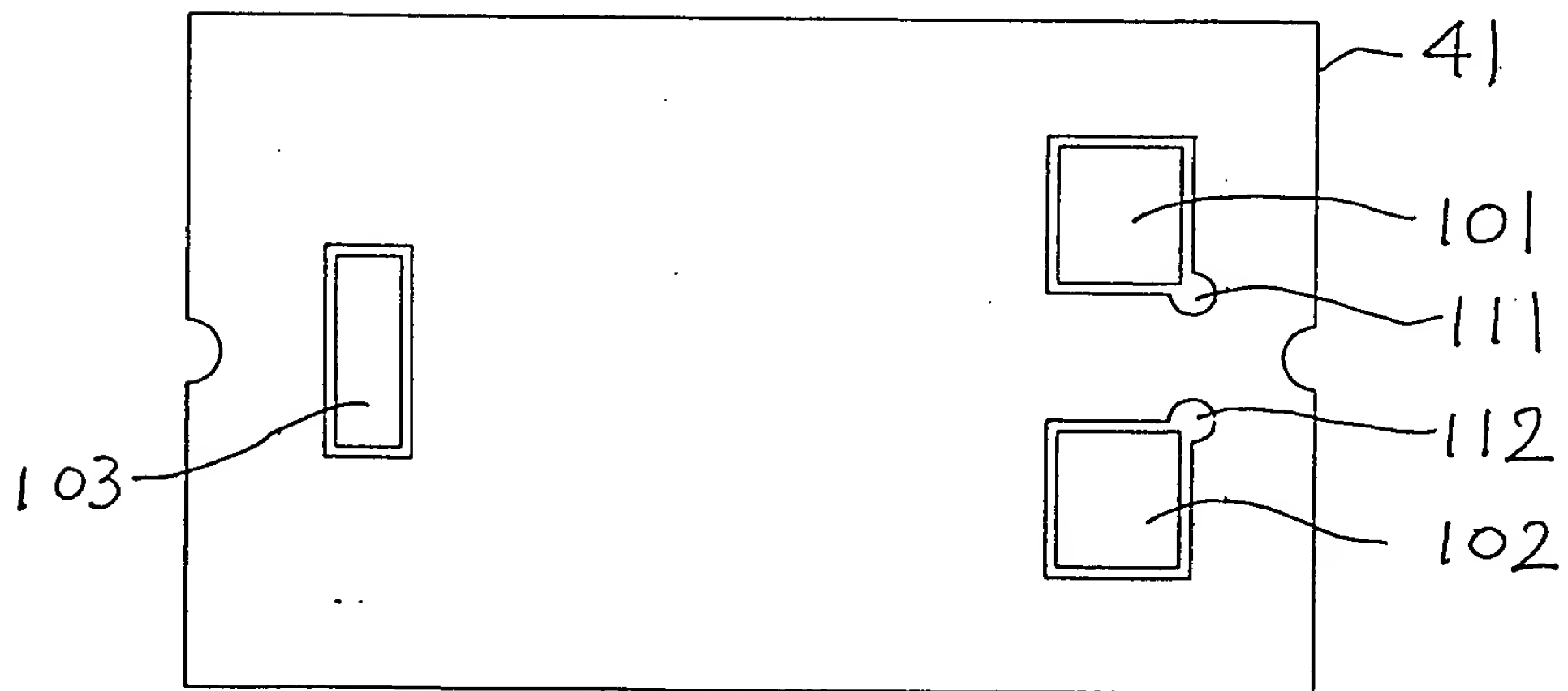


FIG. 16

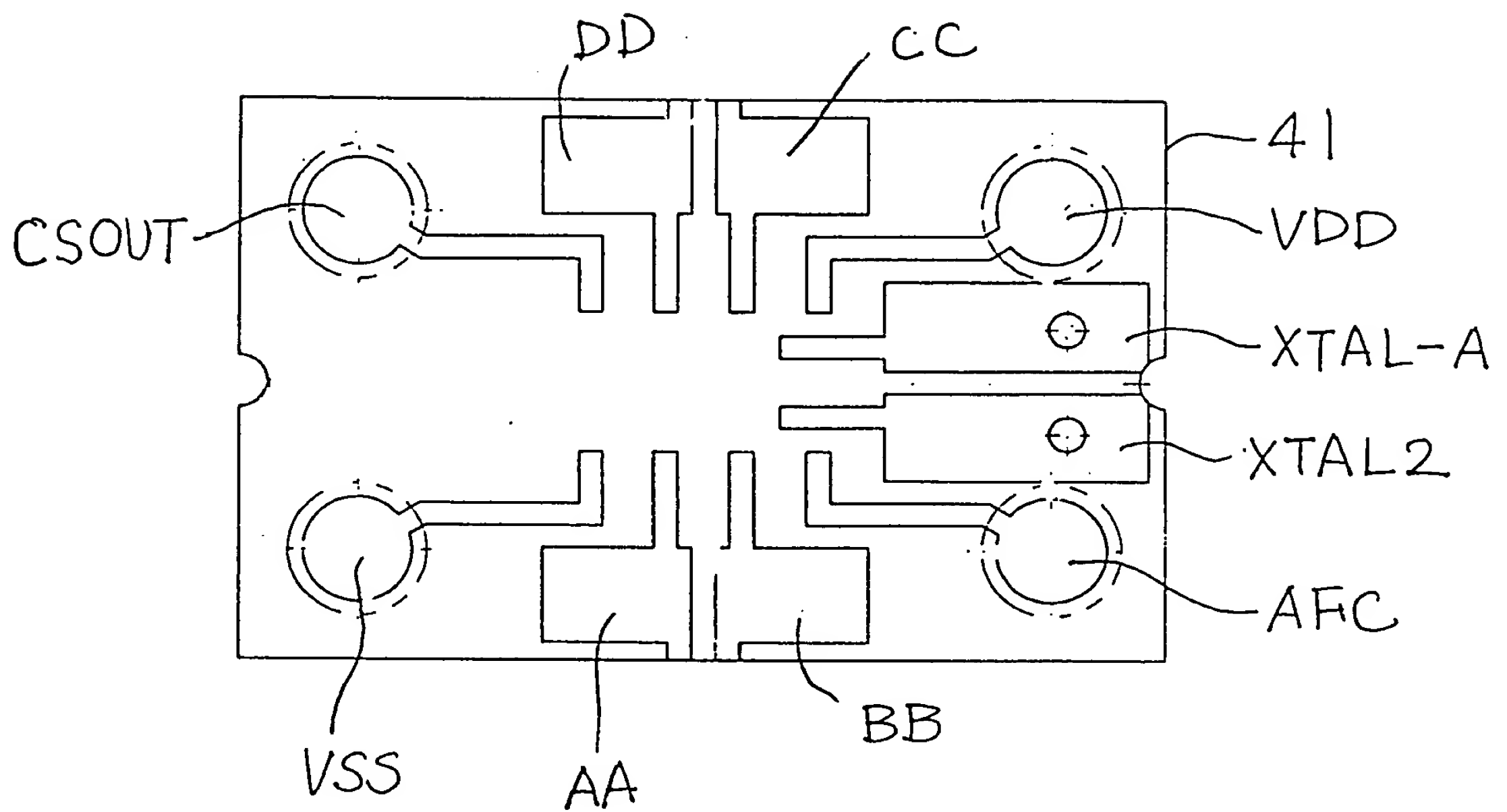


FIG. 17

